REMARKS

Reexamination and reconsideration of this application as amended is requested. By this amendment, Claims 1, 7, 10, 12 and 15 have been amended. Claims 3-6 have been cancelled, without prejudice or disclaimer. After this amendment, Claims 1-2 and 7-15 remain pending in this application.

The Present Invention

The present invention provides a more efficient method for the customization of gate delays that utilizes a VHDL package of array constants. The VHDL package of array constants replaces a significant amount of SDF file declarations for back annotation. The VHDL package of constants is efficient because it only has to be as large as the correlation of the delays, which can be quite significant when delay values are typically clustered around a range of values. Page 18, lines 9-10 of the instant specification. The back annotation process for the gate delays consists merely of resolving constant values for the fixed equations for the delay generics in the VHDL that describe gate behavior for the technology. These delay equations are formulated to depend on just two generics (rise/fall super generics) per gate instance. Page 28, lines 7-9 of the instant specification. The two generics the equations utilize are extracted via a SDF **which is significantly reduced in size.** Page 28, lines 3-6 of the instant specification. Therefore the back annotation process, which is a considerable space and time penalty for large chips in prior art (page 3, lines 12-18 of the instant specification), **is reduced to just two generic back annotations per gate instance.** The instant specification describes a VHDL library method that exploits these savings. Run time binding support of VHDL is utilized to have the constants in the VHDL delay equations resolved at model simulation time, which is a more efficient process than the traditional SDF back annotation of each individual gate delay value. Page 31, line 8-13 of the instant specification.

The instant method of customizing logic gate delays provides both space and time savings. For large chips, the SDF is typically the same size as, or larger than, the chip logic VHDL model, which imparts a huge overhead in storage and processing time in delay customization of a chip during simulation. The correlation of delays (which is the claimed subject matter of co-pending application no. 10/038,209) affords significant savings in the number of delay values that must be specified. This enables innovation in the method defining those delays, as well as enabling innovation in the method to back annotate those delays to VHDL model.

In each of the cited references, the overhead of SDF lexical scan/parse, delay extraction, and application of delay to generic variables in the simulation model VHDL is required for **each** individual delay defined in **each** gate instance. All of this data must be described in the SDF, which amounts to a huge amount of data for large chips.

The present invention utilizes a VHDL equation, where the equation resolves to a constant value, once all constants are resolved at simulation time. The annotation of just two generics per gate instance significantly reduces the processing time and space required for back annotation. The linear relationship of two generics per gate instance holds no matter what size chip is simulated. This allows chips to participate in simulation, which may not have been able to be simulated due to size limitations or performance concerns directly attributable to SDF processing. The instant specification discloses an embodiment of a VHDL library method to realize these savings. In summary, the novelty of the claimed invention is a method to customize a generic chip VHDL gate library with specific delay values in a more efficient manner (significant space and processing time savings) than in the prior art.

Claims Rejection under 35 U.S.C. § 112, first paragraph

(5) The Examiner rejected Claim 3 under 35 U.S.C. § 112, first paragraph, as failing

to comply with the enablement requirement.

Claim 3 has been cancelled from the application.

Claims Rejection under 35 U.S.C. § 112, second paragraph

(6) The Examiner rejected Claims 1-15 under 35 U.S.C. § 112, second paragraph, as failing to set forth the subject matter which applicants regard as their invention.

Specifically, with regard to claims 1, 6, 7, 10, 12, & 15, the Examiner states that the method claimed does not claim the invention as disclosed in the specification. The Applicants respectfully disagree with the Examiner's conclusion.

Claims 1 and 10 have been amended to further clarify that which the applicants regard as their invention. Claims 1 and 10 recite, *inter alia*:

> Storing in a memory a tpd_super_rise generic declaration and a tpd_super_fall generic declaration for every VHDL gate model in a VHDL technology library;
> initializing other generic variables corresponding to every VHDL gate model in the VHDL technology library to an equation representing a correlation policy; and
> storing in a memory an updated VHDL technology library including
> the tpd_super_rise generic declaration and the tpd_super_fall generic declaration for every VHDL gate model, and
> the initialized other generic variables.

Applicants submit that each and every element of the claims is found in the specification as originally filed. The step of *storing a tpd_super_rise generic declaration and a tpd_super_fall generic declaration for every VHDL gate model in a VHDL technology library* is described on page 28, line 8 through page 29, line 5 of the instant specification. The step of *initializing other generic variables corresponding to every VHDL gate model in the VHDL technology library to an equation representing a*

correlation policy is described on page 31, lines 17-22 of the instant specification. Finally, the step of *storing an updated VHDL technology library including the tpd_super_rise generic declaration and the tpd_super_fall generic declaration for every VHDL gate model, and the initialized other generic variables* is described on page 29, line 21 through page 30, line 5.

Claim 7 recites limitations that are substantially similar to limitations recited for claims 1 and 10. Support for the limitations recited in claim 7 can be found in the same locations of the instant specification as the corresponding limitations recited for claims 1 and 10, as identified above.

In view of the remarks above, Applicants believe that the rejection of Claims 1, 7, and 10, under 35 U.S.C. § 112, second paragraph, as discussed above, has been overcome. Applicants request that the Examiner withdraw the rejection of Claims 1, 7, and 10.

Claim 6 has been cancelled.

Claim 12 has been amended to add the limitation "*using a VHDL package embedded with correlation delay data*" as suggested by the Examiner on page 4 of the Office action for now cancelled claim 3, which is similar to claim 12. No new matter was added.

Claim 15 recites, *inter alia*:

> using a tpd_super_rise generic declaration and a tpd_super_fall generic declaration, each generic declaration comprising at least one pointer, for every VHDL gate model in a VHDL technology library to index into a 3-dimensional variable data array structure comprising delay values; and
>
> resolving the pointers when VHDL modules are linked together.

Applicants submit that each and every element of claim 15 is found in the specification as originally filed. The step of *using a tpd_super_rise generic declaration and a tpd_super_fall generic declaration, each generic declaration comprising at least one pointer, for every VHDL gate model in a VHDL technology library to index into a 3-dimensional variable data array structure comprising delay values* is found on page 28, lines 2-20 and the step of *resolving the pointers when VHDL modules are linked together* is found on page 35, lines 8-11 of the instant specification.

In view of the remarks above, Applicants believe that the rejection of Claims 1, 7, 10, 12, and 15 under 35 U.S.C. § 112, second paragraph, as discussed above, has been overcome. Claims 2, 8, 9, 11, 13, and 14 depend from independent claims 1, 7, 10, 12, and 15 and are also believed to recite in allowable form. Applicants kindly request that the Examiner withdraw the rejection of Claims 1-15.

Claim Rejections - under 35 USC § 101

(8) The Examiner rejected Claims 1-6 & 10-11 under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Specifically, the Examiner states that the method of claim 1 is drawn to non-statutory descriptive material. Additionally, the Examiner states that the method of claim 1 is merely drawn to a mental process.

Claim 1 has been amended, per the Examiner's suggestion, to be a *computer implemented* method. Claim 1 has been additionally amended to clarify that data is being stored in *memory*, which is a computer readable medium. It is therefore submitted that claim 1 meets the requirements of 35 U.S.C. § 101 and MPEP §§ 2106, 2111.

Claims 3-6 have been cancelled, without prejudice or disclaimer.

The Examiner states that claim 10 has been rejected because it discloses a computer readable medium that is not defined to be a tangible medium.

Claim 10 has been amended to add the following preamble:

> A computer program product for updating a VHDL Technology Library for efficient customization of chip gate delays, the computer program product comprising:
> a storage medium readable by a processing circuit and storing instructions for execution by the processing circuit for performing a method comprising

The language added to claim 10 recites a tangibly embodied computer readable medium and renders the claim patentable under 35 U.S.C. § 101.

In view of the amendments and remarks above, Applicants believe that the rejection of Claims 1 and 10 under 35 U.S.C. § 101, as discussed above, has been overcome. Claims 2 and 11 depend from independent claims 1 and 10 and are also believed to be allowable. Applicants request that the Examiner withdraw the rejection of Claims 1-6 & 10-11.

Claim Rejections - 35 USC § 103

(9) The Examiner rejected Claims 1-5 and 10-14 under 35 U.S.C. 103(a) as being unpatentable over IEEE Standard for VITAL ASIC Modeling Specification—IEE Std 1076.4-1995 (Std1076 hereafter), in view of Standard Delay Format Specification Version 2.1 by Open Verilog International (OVI2.1 hereafter).

Claims 1 and 10 recite, *inter alia*:

> Storing in a memory a tpd_super_rise generic declaration and a tpd_super_fall generic declaration for every VHDL gate model in a VHDL technology library;

initializing other generic variables corresponding to every VHDL gate model in the VHDL technology library to an equation representing a correlation policy; and

storing in a memory an updated VHDL technology library including

the tpd_super_rise generic declaration and the tpd_super_fall generic declaration for every VHDL gate model, and

the initialized other generic variables.

As the Examiner correctly recognizes on page 10 of the Office Action, Std 1076 does not teach specifically the correlation policy associated with the delay and cites OVI2.1 for teaching this matter.

However, the scope of correlation taught by the OVI2.1 reference is limited to a single instance of a logic gate. OVI2.1 3-10 to 3-12. In contrast, in the present invention, the SDF size reduction is based on the correlation of disparate delay values of multiple logic gates. This correlation process produces a reduced set of delays, by performing delay correlation analysis across an entire chip as represented in the SDF file. The correlation process correlates delays according to a policy of combining common delays for a common delay generic name such that the same delays can be reused regardless of the chip size. This method provides the advantage that the SDF size reduction utilizing this technique, will scale well with increased chip size, resulting in a larger percentage size reduction for the larger, and more problematic, chip sizes. Page 16, lines 7-10 of the instant specification. Therefore, the correlation taught in the cited references is not similar and not performed for the same purpose and in the same way as in the present invention.

Claims 3-5 have been cancelled, without prejudice.

Claims 10 and 11 contain limitations similar to limitations recited for claims 1 and 2, and, therefore, distinguish over the art for the same reasons claims 1 and 2 distinguish over the prior art.

Regarding claim 12, as the Examiner correctly recognizes in the analysis of claim 3 on page 11 of the Office Action, the array in Std1076 is not 3 dimensional.

The presently claimed invention, as recited for claim 12, uses the 3-dimensional array for efficiently indexing and retrieving the values from a data structure (1104). This structure is also used to bind the correlated delay values to the VHDL technology library (306) via a VHDL package (a VHDL construct that allows for sharing of common data items). A 3-dimensional variable array structure is utilized to most efficiently specify correlated delays. The z-axis of the inventive data structure represents a set of **common** blocks for each logical topology (e.g., AND2_LOW (low power), AND2_MED (medium power), AND2_HIGH (high power) are one set of common blocks: AND2_NEW). Each entry on this axis depicts logic gates with a **common** topology (same amount and type of delays). Page 21, lines 2-12 of the instant specification.

As explained in detail above, the correlation in the present invention is not similar and not performed for the same purpose and in the same way as in the cited references. The scope of correlation taught by the OVI2.1 reference is limited to a single instance of a logic gate. The 3D variable array structure of the present invention is used for efficient representation of correlation delays for a particular correlation set.

Accordingly, in view of the remarks above, since neither the Std1076, the OVI2.1, nor any combination of the two cited references, teaches, anticipates, or suggests, the presently claimed correlation policy, Applicants believe that the rejection of Claims 1-2 and 10-14 under 35 U.S.C. 103(a) has been overcome. The Examiner should withdraw the rejection of these claims.

(10) The Examiner rejected Claims 6 and 15 under 35 U.S.C. 103(a) as being unpatentable over IEEE Standard for VITAL ASIC Modeling Specification—IEE Std 1076.4-1995 (Std1076 hereafter), in view of IEEE Standard for Integrated Circuit (IC) Delay and Power Calculation System—IEEE Std 1481-1999 (Std1481 hereafter).

Claim 6 has been cancelled, without prejudice.

Claim 15 recites, *inter alia*:

> using a tpd_super_rise generic declaration and a tpd_super_fall generic declaration, each generic declaration comprising at least one pointer, for every VHDL gate model in a VHDL technology library to index into a 3-dimensional variable data array structure comprising delay values; and
>
> resolving the pointers when VHDL modules are linked together.

In each of the cited references, the overhead of SDF lexical scan/parse, delay extraction, and application of delay to generic variables in the simulation model VHDL is required for **each** individual delay defined in **each** gate instance. All of this data must be described in the SDF, which amounts to a huge amount of data for large chips.

The presently claimed invention utilizes a back annotation process for the gate delays which consists merely of resolving constant values for fixed equations for the delay generics in the VHDL that describe gate behavior for the technology. These delay equations are formulated to depend on just two generics (rise/fall super generics) per gate instance. Page 28, lines 7-9 of the instant specification. The two generics the equations utilize are extracted via a reduced SDF which is significantly reduced in size compared to the original SDF. Page 28, lines 3-6 of the instant specification. Therefore the back annotation process, which is a considerable space and time penalty for large chips in prior art (page 3, lines 12-18 of the instant specification), is reduced to just two generic back annotations per gate instance.

More specifically, in the present invention, two single super generics tpd_super_rise (rise times) and tpd_super_fall (fall times) for a selected instance are built by an SDF **reducer**. Page 28, lines 7-9. Therefore, the data structure "tpd_super" represents a "super generic" value in a **reduced** SDF file that encapsulates all of the delay values for a particular gate.

None of the cited references teach or suggest a reduced SDF file or a "super generic." Therefore, the cited references do not teach or suggest a tpd_super_rise generic declaration and a tpd_super_fall generic declaration, as claimed in claim 15 of the present invention.

In view of the amendments and remarks above, Applicants believe that the rejection of Claim 15 under 35 U.S.C. § 103(a), as discussed above, has been overcome. Applicants request that the Examiner withdraw the rejection of Claim 15.

(11) The Examiner rejected Claims 7-9 under 35 U.S.C. 103(a) as being unpatentable over IEEE Standard for VITAL ASIC Modeling Specification—IEE Std 1076.4-1995 (Std1076 hereafter), in view of IEEE Standard for Integrated Circuit (IC) Delay and Power Calculation System—IEEE Std 1481-1999 (Std1481 hereafter), further in view of Standard Delay Format Specification Version 2.1 by Open Verilog International (OVI2.1 hereafter).

Claim 7 recites, *inter alia*:

> a memory for storing a VHDL technology library and a VHDL technology library modifier, the memory communicatively coupled to the processor/controller, for:
>
> inserting a tpd_super_rise generic declaration and a tpd_super_fall generic declaration for at least one VHDL gate model in the VHDL technology library,
>
> initializing other generic variables in every VHDL gate model in the VHDL technology library to an equation representing a correlation policy, and
>
> storing an updated VHDL technology library including the tpd_super_rise generic declaration and the tpd_super_fall generic declaration for the at least one VHDL gate model, and including the initialized other generic variables.

In the present invention, two single super generics tpd_super_rise (rise times) and tpd_super_fall (fall times) for a selected instance are built by an SDF **reducer**. Page 28,

lines 7-9. Therefore, the data structure "tpd_super" represents a "super generic" value in a **reduced** SDF file that encapsulates all of the delay values for a particular gate.

None of the cited references teach or suggest a reduced SDF file or a "super generic." Therefore, the cited references do not teach or suggest a tpd_super_rise generic declaration and a tpd_super_fall generic declaration, as claimed in claim 15 of the present invention.

Additionally, as the Examiner correctly recognizes on page 10 of the Office Action, Std 1076 does not teach specifically the correlation policy associated with the delay and cites OVI2.1 for teaching this matter.

However, the scope of correlation taught by the OVI2.1 reference is limited to a single instance of a logic gate. OVI2.1 3-10 to 3-12. In contrast, in the present invention, the SDF size reduction is based on the correlation of disparate delay values of multiple logic gates. This correlation process produces a reduced set of delays, by performing delay correlation analysis across an entire chip as represented in the SDF file. The correlation process correlates delays according to a policy of combining common delays for a common delay generic name such that the same delays can be reused regardless of the chip size. This method provides the advantage that the SDF size reduction utilizing this technique, will scale well with increased chip size, resulting in a larger percentage size reduction for the larger, and more problematic, chip sizes. Page 16, lines 7-10 of the instant specification. Therefore, the correlation taught in the cited references is not similar and not performed for the same purpose and in the same way as in the present invention.

Accordingly, in view of the remarks above, since neither the Std1076, the OVI2.1, or the STD1481, nor any combination of the three cited references, teaches, anticipates, or suggests, the presently claimed correlation policy or super generics, Applicants believe that the rejection of Claims 7-9 under 35 U.S.C. 103(a) has been overcome. The Examiner should withdraw the rejection of these claims.

Conclusion

The foregoing is submitted as full and complete response to the Official Action mailed July 14, 2005, and it is submitted that Claims 1-2 and 7-15 are in condition for allowance. Reconsideration of the rejection is requested. Allowance of Claims 1-2 and 7-15 is earnestly solicited.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Applicants acknowledge the continuing duty of candor and good faith to disclose information known to be material to the examination of this application. In accordance with 37 CFR § 1.56, all such information is dutifully made of record. The foreseeable equivalents of any territory surrendered by amendment are limited to the territory taught by the information of record. No other territory afforded by the doctrine of equivalents is knowingly surrendered and everything else is unforeseeable at the time of this amendment by the Applicants and the attorneys.

If the Examiner believes that there are any informalities that can be corrected by Examiner's amendment, or that in any way it would help expedite the prosecution of the patent application, a telephone call to the undersigned at (561) 989-9811 is respectfully solicited.

The Commissioner is hereby authorized to charge any fees that may be required or credit any overpayment to Deposit Account **50-1556.**

In view of the preceding discussion, it is submitted that the claims are in condition for allowance. Reconsideration and re-examination is requested.

Respectfully submitted,

Date: October 14, 2005

By: _____

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